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09/820,512	03/29/2001	David William Boerstler	AUS920000511US1	5447

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Kelly K. Kordzik
Suite 800
100 Congress Avenue
Austin, TX 78701

EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,512	BOERSTLER, DAVID WILLIAM	
	Examiner	Art Unit	
	YOUNG T. TSE	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,12-14 and 24* is/are rejected.

7)☒ Claim(s) *3-11 and 15-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, claim 13 recites a transmission medium; a transmitter coupled to said transmission medium, wherein said transmitter is configured to transmit data in a serial from; and a receiver coupled to said transmission medium and is configured to receive said serial data. The receiver further comprising an oscillator and a retiming mechanism and is considered as the main invention. As pointed out in paragraph 8 of the last Office Action, even without the combination of the second reference Ducariot, claim 13 is unpatentable over Buckner because the data phase alignment circuits 34 are located in a receiver circuit and each of the data phase alignment circuits 34 receives a serial data (DATA_IN), for example, telephony, digital and video data 16 (see col. 3, lines 7-10 and Figure 2). Further, It is also well known to a person skill in the art to realize that a wire-connection receiver is capable of receiving serial data from a transmitter through a transmission medium. Therefore, when Buckner's data phase

alignment circuit 34 of the receiver meets all the claimed subject matter of the receiver circuit as recited in claim 13, it is obvious to one of ordinary skill in the art that the digital and video data is transmitted from other circuitries, for instance, from a transmitter through a transmission medium as recited in claim 13.

With respect to claim 14 (also see claim 2), the Applicant argues Buckner discloses that the outputs from exclusive-NOR gates 110-118 are then provided to complementary MOS (CMOS) transmission gates 120-128, respectively, which are controlled by clock phases and data. Column 5, lines 4-8. There is no language in the cited passage that discloses that transmission gates 120-128 generate particular retiming states. Further, transmission gates 120-128 are not located within data retimer circuit 50 as asserted by the Examiner. Instead, transmission gates 120-128 are located within data decoder 44. See Figure 6a. Thus, Buckner does not disclose all of the limitations of claim 14, and thus Buckner does not anticipate claim 14, as well as claim 2.

Notice, the subject matter of the argument seems not recited in neither claim 14 nor claim 2, for example, claim 14 recites wherein each particular phase of said clock to be asserted to sample said serial data during said period of said serial data corresponds to a particular retiming state. Clearly, as recited in claims 14 and 2, the transmission gates 120-128 do not have to be located within the data retimer circuit 50. As shown in Figure 6a, the outputs of the transmission gates 120-128 are connected to logic circuits 140 to 168 to generate logic or delayed logic states which may considered as particular retiming states since the term "a particular retiming state" is broad which can read on

the outputs of the transmission gates 120-128, the logic circuits 140 to 168, or the combination of the transmission gates 120-128 and the logic circuits 140 to 168.

With respect to claims 12 and 24, each claim recites wherein said oscillator operates at a frequency lower than a data rate of said serial data. Although Buckner does not explicitly show or suggest the relationship about the frequency or data rate between the oscillator and the data stream DATA_IN, Lee teaches that the data and recovered clock provided to the serial to parallel converter 206 will be processed at a much lower rate than the data baud rate to produce synchronized data and clock before the data is transferred to the media access control (MAC) 102 circuitry (see column 5, lines 52-58). Also see paragraph 9 of the last Office Action. Even without the second reference Lee, claims 12 and 24 are unpatentable in view of Buckner. It is also well known to a person skill in the art to realize that a retiming circuit is used to align or synchronize a serial data stream with the frequency or data clock of an oscillator circuit, in this case, the data rate or frequency of the serial data stream and the oscillator is the same, however, when the data rate of the serial data stream is not synchronized (asynchronous) with the frequency of the oscillator, the oscillator operates at the frequency is either lower or higher than the data rate of the serial data stream. Therefore, it would have been obvious to one of ordinary skill in the art that the frequency in Buckner's oscillator 43 could be lower than the data rate of the DATA_IN since the data is an asynchronous data transmitted through an asynchronous data capturer 40. Further, it can be the choice of design for an oscillator to generate clock signals or frequencies at a data rate lower than the data rate of the serial data of a

retiming circuit since an oscillator can generate different degree of data rates or frequencies which is the choice of design depending on the requirements of the invention.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Buckner et al.

Buckner et al. (US Patent No. 5,509,037) (hereinafter "Buckner") discloses a receiver circuit in Figure 2 comprising a plurality of phase alignment circuits 34 for aligning a plurality of serial data with a plurality of clock phases generated from a phase locked loop (PLL) circuit 30 of an internal clock to generate retiming data to a switching matrix 36.

Figure 3 shows the detailed embodiment of the PLL circuit 30 for generating the plurality of the clock phases.

Figure 4 shows the waveforms of the plurality of clock phases, the input of the serial data, and the retiming data of the serial data.

Figure 5 shows the detailed embodiment of one of the plurality of the phase alignment circuits 34 comprising a retiming circuitry 37 and a slip buffer 38.

The retiming circuitry 37 includes an asynchronous data capturer 40 for receiving the serial data and the phases of the internal clock, a data transition decoder 44 for performing the task of determining the occurrence of the data transition with respect to the plurality of clock phases, and a data timer 50 for realigning the captured data of one of the plurality of the clock phases. See column 4, lines 14-41 and column 5, lines 31-34.

The detailed embodiment of both the asynchronous data capturer 40 and the data transition decoder 44 is shown in Figure 6a and the detailed embodiment of the data timer 50 is shown in Figures 6b and 6c.

The slip buffer 38 includes a forward/backward decoder 56, a state machine 58, and a data path selector 64.

The detailed embodiment of the forward/backward decoder 56, the state machine 58, and the data path selector 64 is shown in Figures 7a and 7b.

With respect to claim 2, the phases of the internal clock are generated by the voltage controlled oscillator (VCO) 43 of the PLL circuit 30; the retiming circuit 34 includes the asynchronous data capturer 40 for receiving the serial data and the phases of the internal clock and the data transition decoder 44 the data timer 50 which may also includes the data path selector 62 operable to reduce timing uncertainties in the serial data by outputting a value of the serial data sampled at a particular phase of the internal clock. Wherein each data phase alignment circuitry 34 receives phases $\Phi 1$- $\Phi 5$ of the clock signal, the serial data, and aligns the data with a selected phase of the clock signal. See column 3, lines 34-36. Further, the data generated by the data timer 50

corresponds to a particular retiming state, which may be generated, for example, by the CMOS transmission gates 120-128, the logic circuits 14-168, or the combination of the CMOS transmission gates 120-128 and the logic circuits 14-168. See column 5, lines 4-8.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckner et al. in view of Ducaroir et al..

With respect to claims 13 and 14, Buckner discloses all the claimed subject matter as recited in claim 2 and discussed in paragraph 3 above. However, Buckner

fails to show or suggest that the receiver circuit receives the serial data from a transmission medium transmitted by a transmitter comprising a parallel to serial converter for converting the serial data to the transmission medium.

Ducaroir et al. (U.S. Patent No. 6,331,999 B1) (hereinafter "Ducaroir") discloses a serial data transceiver circuit 59 in Figure 7 comprising a transmitter circuit having a parallel to serial converter to convert a parallel input data to a serial data stream and a receiver circuit to receive the serial data stream to parallel output, recover a transmit clock signal used to transmit the serial data from the serial data stream to generate a timing signal based upon the recovered transmit clock, samples the serial data stream using the timing signal in order to recover the data stream from the serial data stream, align the serialized data into parallel units, and provide the resulting parallel data at the received data output port. See the abstract.

Therefore, it would have been obvious to one of ordinary skill in the art that the serial data received in Buckner's receiver circuit is transmitted from a parallel to serial converter circuit of a transmitter through a transmission medium in order to recover a transmitted clock by a receiver as taught by Ducaroir.

7. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckner et al. in view of Lee et al.

As applied to claim 2 and claim 13 discussed in paragraphs 3 and 6 above. Although Buckner does not show or suggest the relationship of the data rate between the serial data and the clock signal that the oscillator 43 operates at a frequency lower than a data rate of the serial data. It appears to be well known to a person skill in the

art that the frequency generated from one of the phases Φ1- Φ5 by the oscillator 43 is lower than the data rate of the serial data since the oscillator 43 has divided the internal clock into five different clock phases and the data stream of the retiming circuit is asynchronous data.

Even it is not well known to a person skill in the art as discussed above, Lee et al. (U.S. Patent No. 6,266,799) (hereinafter "Lee") discloses a data/clock recovery system 100 in Figure 1 comprising a transmitter circuit 108 for transmitting a serial data to a receiver circuit 110 through a transmission medium.

Figure 2 shows the detailed embodiment of the receiver circuit 110 having a multi-phase clock generator 204 for generating a plurality of clock phases, a multi-phase data clock recovery unit 110a for recovering the serial data and the plurality of clock phases into recovery clocks and data to a serial to parallel converter 206.

Lee teaches that the data and recovered clock provided to the serial to parallel converter 206 will be processed at a much lower rate than the data baud rate to produce synchronized data and clock before the data is transferred to the media access control (MAC) 102 circuitry. See column 5, lines 52-58.

Therefore, it would have been obvious to one of ordinary skill in the art to generate a frequency in Buckner's oscillator 43 lower than the data rate of the serial data as taught by Lee for the purpose of saving power or synchronize data and clock before the data is transferred to other circuitry.

Allowable Subject Matter

8. Claims 3-11 and 15-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Thursday and alternative Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The Central FAX Number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YOUNG T. TSE
Primary Examiner
Art Unit 2637